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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)

B.Tech II Year I Semester Supplementary Examinations December-2021
DIGITAL SYSTEM DESIGN

(Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 60

PART-A

(Answer all the Questions 5 x 2 = 10 Marks)

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|---|---|---|----|----|
| 1 | a | What is meant by parity bit? | L1 | 2M |
| | b | Mention the expressions for difference and borrow of Full Subtractor. | L2 | 2M |
| | c | Define Flip-flop. What are the applications of FF | L1 | 2M |
| | d | What are the advantages of flash memory? | L1 | 2M |
| | e | Give any two differences between different modeling styles of VHDL. | L1 | 2M |

PART-B

(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

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|---|---|--|----|----|
| 2 | a | Convert the given decimal number 234 to binary, octal, hexadecimal and BCD equivalent. | L1 | 5M |
| | b | Convert the following.
i. $(BC)_{16} = ()_{10}$ ii. $(2314)_8 = ()_{10}$ iii. $(1000011)_2 = ()_{10}$
iv. $(647)_{10} = ()_{16}$ | L1 | 5M |

OR

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|---|---|--|----|----|
| 3 | a | Explain about the Binary Codes. | L1 | 5M |
| | b | Simplify the following Boolean functions to minimum number of literals.
i) $F = xy + x'z + yz$
ii) $F = x'y'z + x'yz + xy'$
iii) $F = (x+y)'(x'+y')$
iv) $F = xy + xy' + x'y$
v) $F = (BC' + A'D)(AB' + CD')$ | L1 | 5M |

UNIT-II

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|---|---|----|-----|
| 4 | | L2 | 10M |
| | Simplify the following Boolean function for minimal SOP & POS form using K-map. $F(A, B, C, D) = \Sigma(0, 1, 2, 5, 8, 9, 10)$
ii. $F(A, B, C, D) = \pi(1, 3, 5, 7, 12, 13, 14, 15)$ | | |

OR

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|---|---|---|----|----|
| 5 | a | What is Encoder? Design an octal to binary Encoder. | L3 | 5M |
| | b | Design & Implement an 8:1 Multiplexer. | L3 | 5M |

UNIT-III

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|---|---|---|----|----|
| 6 | a | Implement D-FF using JK FF with its truth table. | L4 | 5M |
| | b | Draw the basic flip-flop circuit with NOR gates. Explain its operation. | L2 | 5M |

OR

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|---|---|--|----|----|
| 7 | a | Explain the difference between Ring and Johnson counters with neat sketch. | L4 | 6M |
| | b | Design a 4-bit synchronous up counter using JK flip-flops. | L2 | 4M |

UNIT-IV

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|---|---|--|----|----|
| 8 | a | Explain about TTL to CMOS interfacing. | L4 | 6M |
| | b | Compare TTL, ECL and CMOS. | L1 | 4M |

OR

- 9 a Derive the PLA programming table for the combinational circuit that squares a 3-bit number. L2 5M
b Compare three combinational circuits: PLA, PAL and ROM. L1 5M
- UNIT-V**
- 10 a Write a VHDL program for a 4X1 MUX. L4 5M
b Discuss in detail about Data Flow design elements. L4 5M
- OR**
- 11 a Design a logic circuit and write a VHDL program to add 3 bit numbers. L5 5M
b Explain about Simulation and Synthesis processes in VHDL. L2 5M

END